

FEATURES

- Display Format: 320 × 240
- Overall Dimensions:
148 (W) × 96 (H) × 8 max (D) mm
- Active Area: 100 (W) × 76 (H) mm
- Dot Pitch: 0.28 (W) × 0.28 (H) mm

DESCRIPTION

The SHARP LM32P10 Passive Matrix Color LCD consists of 320 × 240 dots with a backlight system which uses a cold cathode fluorescent tube (CCFT). The LCD also consists of a TSTN-type negative panel.

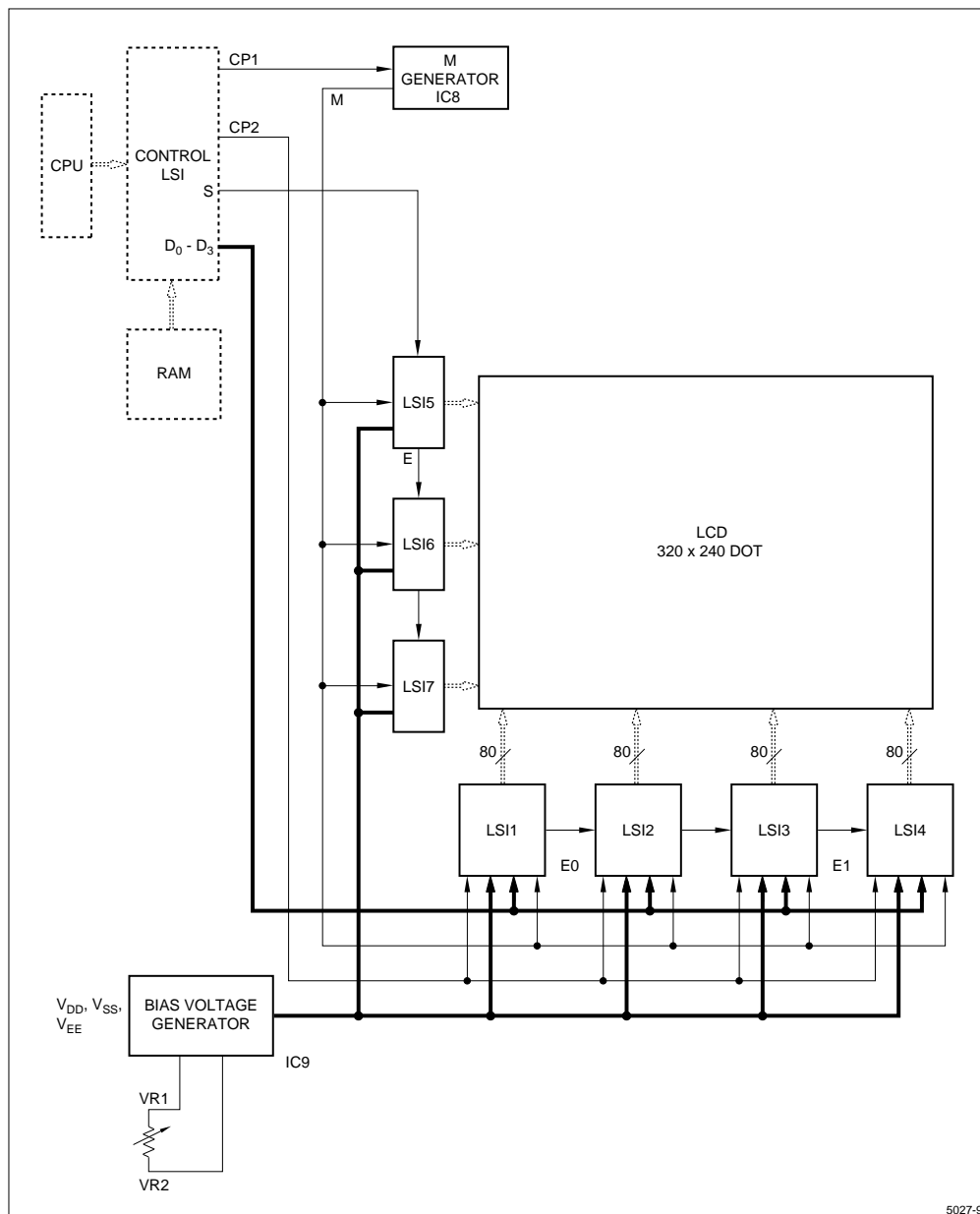


Figure 1. LM32P10 Block Diagram

MECHANICAL SPECIFICATIONS

PARAMETER	SPECIFICATIONS	UNIT	NOTE
Outline Dimensions	148 (W) × 96 (H) × 8 max (D)	mm	1
Effective Viewing Area	100 (W) × 76 (H)	mm	–
Display Format	320 (W) × 240 (H) Full Dot	–	–
Dot Size	0.28 (W) × 0.28 (H)	mm	–
Dot Spacing	0.02	mm	–
Character Color	White	–	2
Background Color	Black	–	2
Weight	Approximately 140	g	–

NOTES:

- Excludes the mounting tab.
- Due to the characteristics of the LC material, the colors vary with environmental temperature.
- Negative-type display:
Display data 'H': Dots ON: White
Display data 'L': Dots OFF: Black

ABSOLUTE MAXIMUM RATINGS ($t_A = 25^\circ\text{C}$)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{DD} - V_{SS}$	Supply Voltage (Logic)	0	6.0	V
$V_{DD} - V_{EE}$	Supply Voltage (LCD Drive)	0	30.0	V
V_{IN}	Input Voltage	0	V_{DD}	V
VCCFT	Supply Voltage (CCFT)	0	1500	V_{RMS}
ICCFT	Supply Current (CCFT)	0	6.5	mA_{RMS}

ENVIRONMENTAL CONDITIONS

ITEM	TSTG		TOPR		CONDITION	NOTE
	MIN.	MAX.	MIN.	MAX.		
Ambient Temperature	-20°C	+60°C	0°C	+45°C	–	–
Humidity	–		–		No condensation	1
Vibration	–		–		3 Directions (X/Y/Z)	2
Shock	–		–		6 Directions ($\pm X/\pm Y/\pm Z$)	3

NOTES:

- $t_A \leq 40^\circ\text{C}$, 90% RH maximum.
 $t_A > 40^\circ\text{C}$, Absolute humidity less than $t_A = 40^\circ\text{C}$ at 90% RH.
- These test conditions are in accordance with IEC 68-2-6.
Two hours for each direction of X/Y/Z (six hours total).

Frequency	10 Hz to 55 Hz
Vibration Width	1.5 mm
Interval	10 Hz to 55 Hz to 10 Hz/1.0 min.

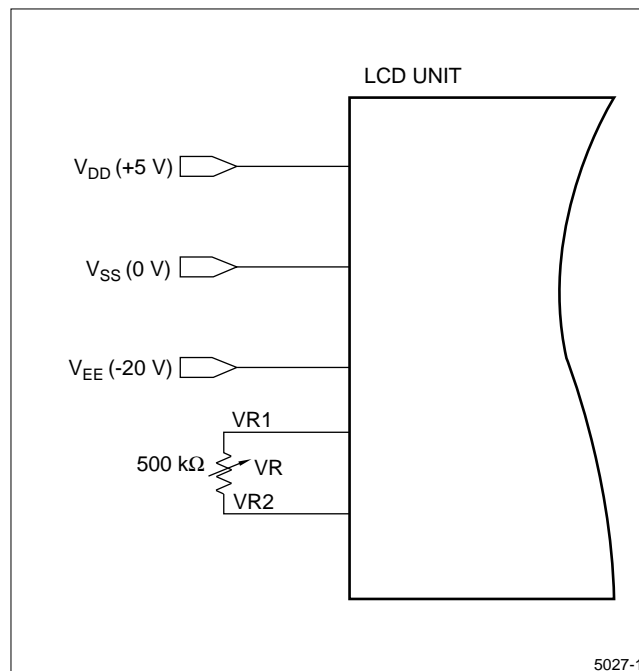
- Acceleration: 490 m/s^2 (50G)
Pulse width: 11 ms
Three times for each direction of $\pm X/\pm Y/\pm Z$.

ELECTRICAL CHARACTERISTICS ($t_A = 25^\circ\text{C}$, $V_{DD} = 5.0\text{ V} \pm 5\%$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITION	NOTE
$V_{DD} - V_{SS}$	Supply Voltage (Logic)	4.75	5.0	5.25	V	–	
$V_{EE} - V_{SS}$	Supply Voltage (LCD Drive)	-21.0	-20.0	-19.0	V	$V_{DD} = 5.0\text{ V}$	1
V_{IN}	Input Signal Voltage	$0.8 V_{DD}$	–	V_{DD}	V	'H' Level	
		0	–	$0.2 V_{DD}$	V	'L' Level	
I_{IL}	Input Leakage Current	–	–	20	μA	'H' Level	
		-20.0	–	–	μA	'L' Level	
I_{DD}	Supply Current (Logic)	–	9	18	mA	$V_{DD} = 5.0\text{ V}$ $V_{EE} = -20.0\text{ V}$ $VR = 250\text{ k}\Omega$ $F = 80\text{ Hz}$	2
I_{EE}	Supply Current (LCD Drive)	–	7	14	mA		
P_{DLCD}	Power Consumption (LCD)	–	185	370	mW		
V_{FTS}	Start Voltage (B/L)	–	–	480	V_{RMS}	Inverter LM000106 Input Voltage 12 V Adjust Resistor 20 k Ω	
V_{FTL}	Supply Voltage (B/L)	225	250	275	V_{RMS}		
I_{FT}	Supply Current (B/L)	4	5	6	mA_{RMS}		
P_{DFT}	Power Consumption (B/L)	–	1.25	–	W		

NOTES:

1. The viewing angle θ that obtains the maximum contrast can be set by adjusting variable resistors between VR1 and VR2.
2. Display high frequency pattern (Figure 2).

**Figure 2. Display High Frequency Pattern**

INTERFACE SIGNALS

CN1 ¹

PIN NUMBER	SYMBOL	PARAMETER	LEVEL
1	S	Scan Start-Up Signal	H
2	CP1	Input Data Latch Signal	H → L
3	CP2	Data Input Clock Signal	H → L
4	V _{DD}	Power Supply For Logic and LCD (+5 V)	–
5	V _{SS}	Ground Potential (GND)	–
6	V _{EE}	Power Supply For LCD	–
7	D ₀	Display Data Signal	H (ON), L (OFF)
8	D ₁		
9	D ₂		
10	D ₃		
11	VR1	LCD Contrast Adjust (A)	–
12	VR2	LCD Contrast Adjust (B)	–

NOTE:

- Connector used: 52103 - 1217 (Molex)
Mating cable: 1.0 mm pitch, 12 pins F.F.C.

CN2

PIN NUMBER	SYMBOL	PARAMETER
1	VFT1	Power Supply for CCFT Backlight
2	VFT2	Power Supply for CCFT Backlight

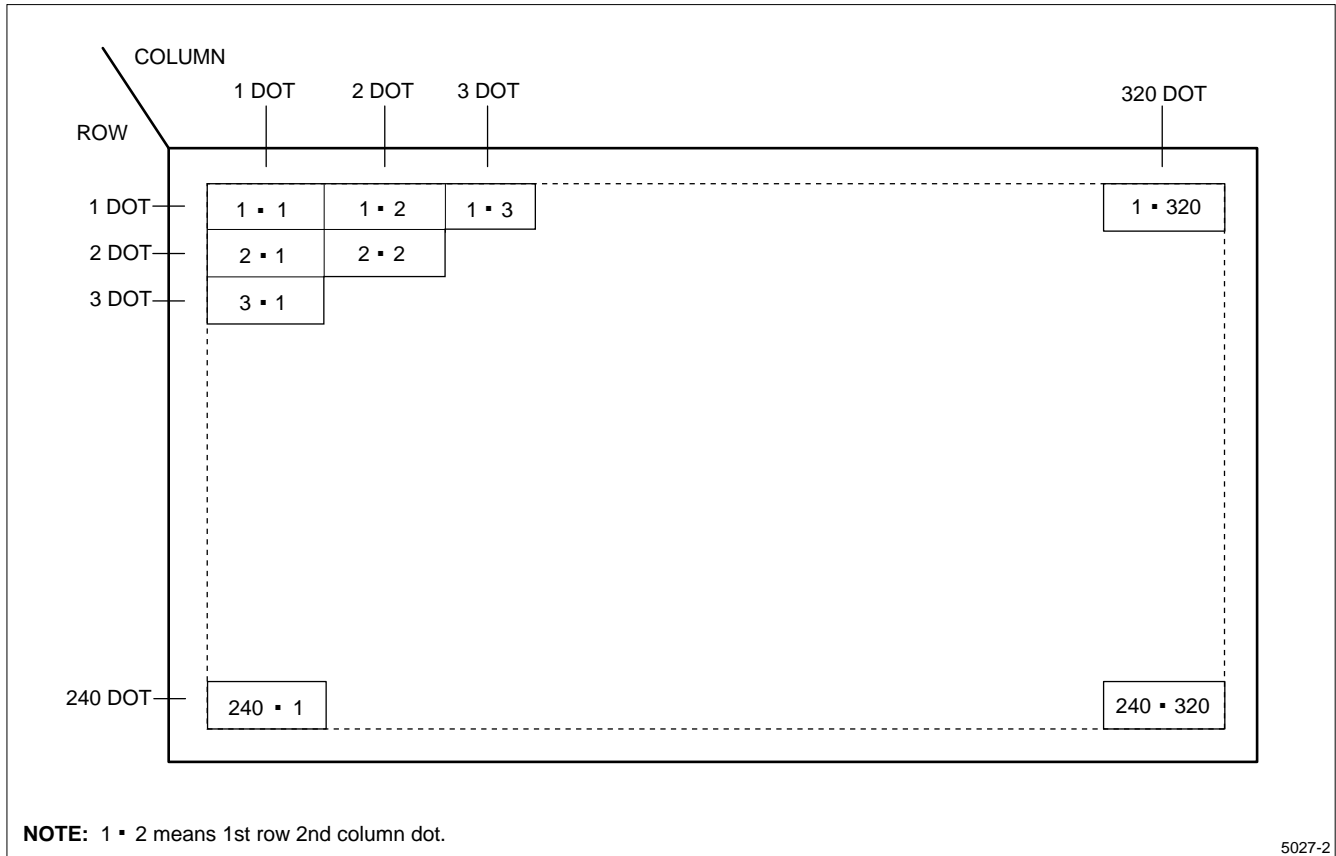


Figure 3. Dot Chart of Display Area

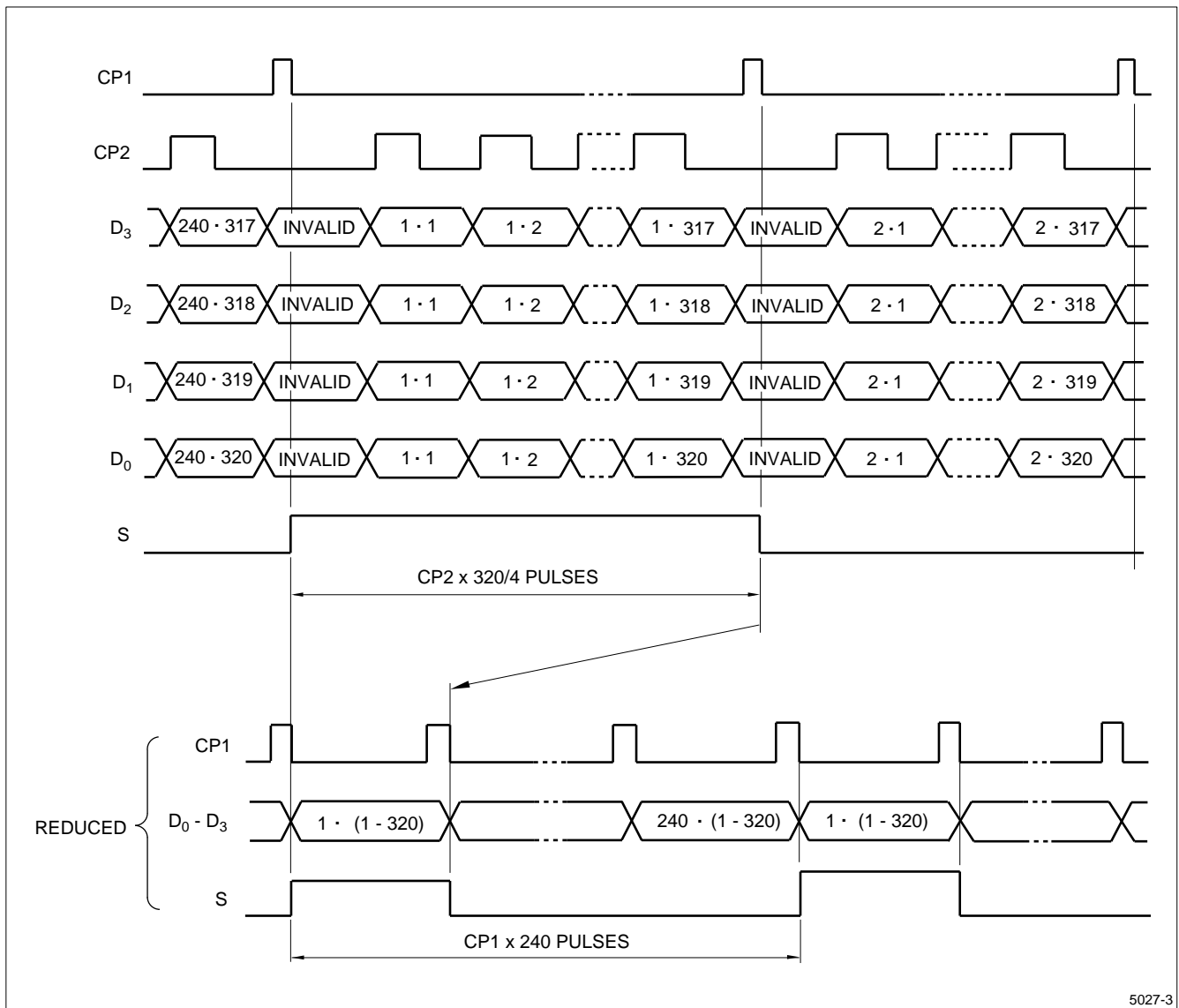


Figure 4. Data Input Timing Chart

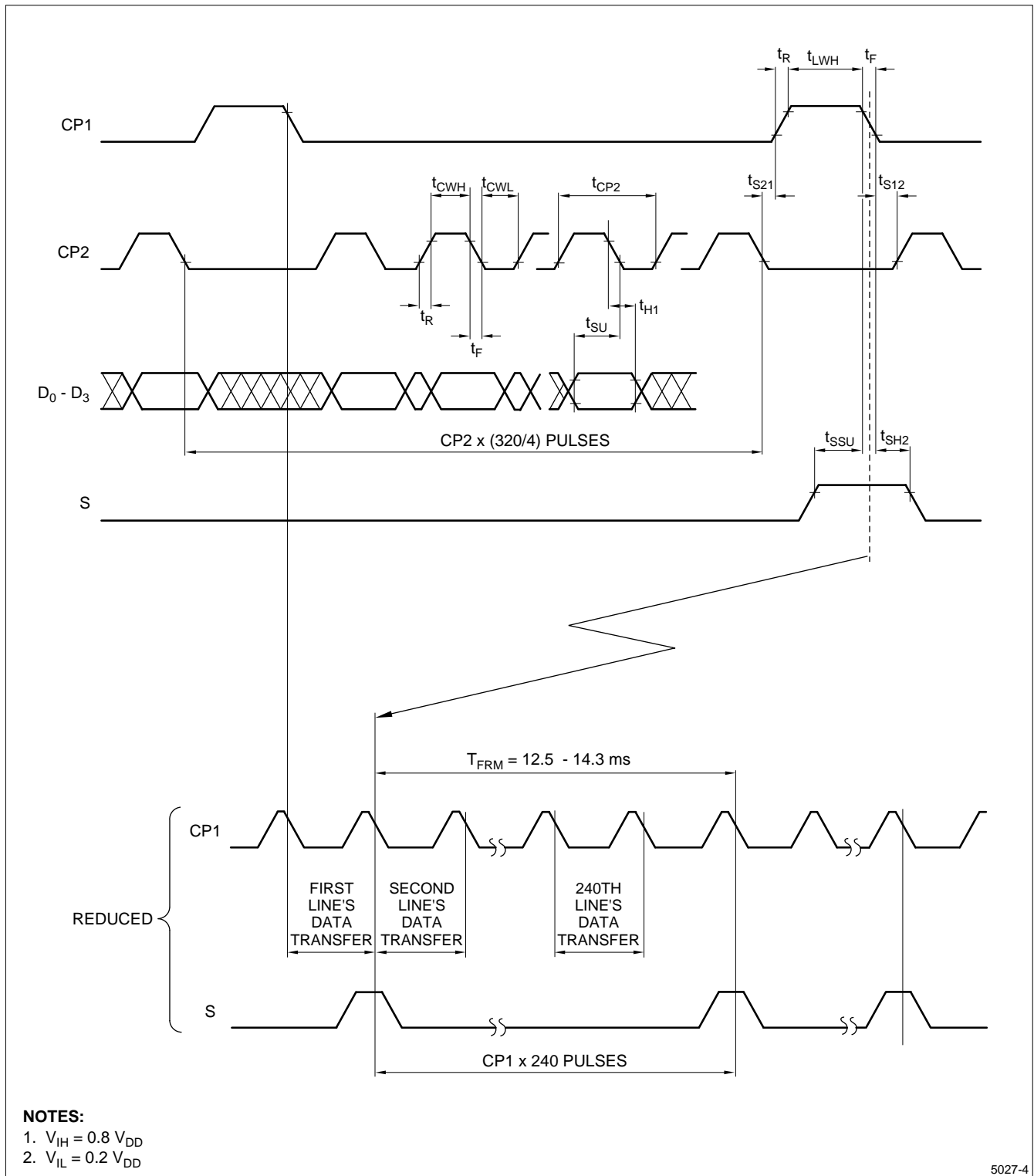


Figure 5. Interface Timing Chart

INTERFACE TIMING RATINGS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
t _{FRM}	Frame Cycle	12.5	–	14.3	s
t _{CP2}	CP2 Clock Cycle	152	–	–	ns
t _{CWH}	'H' Level Clock Width	100	–	–	ns
t _{CWL}	'L' Level Clock Width	100	–	–	ns
t _{LWH}	'H' Level Latch Clock Width	100	–	–	ns
t _{SU}	Data Setup Time	80	–	–	ns
t _{HI}	Data Hold Time	80	–	–	ns
t _R , t _F	Clock Rise/Fall Time	–	–	50	ns
t _{SSU}	S Signal Data Setup Time	100	–	–	ns
t _{SH2}	S Signal Data Hold Time	100	–	–	ns

UNIT DRIVING METHOD

Circuit Configuration

Figure 1 shows the block diagram of the Unit's circuitry.

Display Face Configuration

The display face electrically consists of a signal display segment of 320×240 dots.

Input Data and Control Signal

The LCD driver is 80 bits LSI, consisting of shift register, latch circuits, and LCD driver circuits.

Display data which is externally divided into data for each row (320 dots) is sequentially transferred in the form of 4-bit parallel data through shift registers by Clock Signal CP2 from the left top of the display face.

When data of one row (320 dots) has been input, they are latched in the form of parallel data for 320 lines of signal electrodes by Latch Signal CP1. Then the corresponding drive signal is transmitted to the 320 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal S is transferred from the scan signal driver to the first row of scan electrodes, and the contents of the data signals are displayed on the first row of the upper and lower half of the display face according in the combinations of voltages applied to the scan and signal electrodes of the LCD.

While the first rows of data are being displayed, the second rows of data are entered. When 320 dots of data have been transferred, then latched, on the falling edge of CP1 clock, the display face proceeds to the second rows of display.

Such data input is repeated up to the 240th row of each display segment, from upper to lower rows, to complete one frame of display using the time-sharing method. Then data input proceeds to the next display face. Scan start-up signal S generates scan signal to drive horizontal electrodes. To avoid flickering, drive the unit at 70 – 80 Hz/frame.

Because of the characteristics of the CMOS driver LSI, the power consumption of the unit goes up as the operating frequency CP2 increases. Thus the driver LSI applies the system of transferring 4-bits parallel data through the four lines of shift registers to reduce the data transfer speed CP2. This system minimizes power consumption of the unit.

In this circuit configuration, 4-bit display data are input to data input pins $D_0 - D_3$.

The LCD unit also adopts a bus line system for data input to minimize the power consumption. In this system, the data input terminal of each driver LSI is activated only when relevant data input is fed.

Data input for column electrodes of both the upper and the lower display segment and chip select of driver LSI are made as follows:

- The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI of the right side is selected when 80 dots data (20 CP2) is fed. This process continues sequentially until data is fed to the driver LSI at the right end of the display face.
- This process is immediately followed at the column drivers LSI's of both the upper and the lower display segments. Thus, data input for both the upper and the lower display segments must be fed through 4-bit bus line sequentially from the left end of the display face.

Since this graphic display unit contains no refresh RAM, it requires data and timing pulse inputs even for static display.

OPTICAL CHARACTERISTICS ($V_{DD} = 5.0\text{ V}$, $t_A = 25^\circ\text{C}$)

The following specifications show the optical characteristics when the viewing angle obtaining the maximum contrast (ϕ) is adjusted to 0 degrees.

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE	
$\theta_2 - \theta_1$	Viewing Angle Range	$\phi = 180^\circ$ $C_0 \geq 4.0$	40	—	—	degrees	1	
θ_1			—	—	-20			
θ_2		$\theta_1 < \theta_2$ $C_0 = 4.0$	15	—	—			
$\theta_2 - \theta_1$			$\phi = 270^\circ$ $\theta_1 < \theta_2$	$C_0 \geq 4.0$	45			—
θ_1		$C_0 = 4.0$		—	—			-20
θ_2		20	—	—				
C_0	Contrast Ratio	$\theta = 0^\circ, \phi = 180^\circ$	8.0	18.0	—	—	2	
t_R	Response Speed – Rise	$\theta = 0^\circ, \phi = 180^\circ$	—	200	300	ms	3	
t_D	Response Speed – Decay	$\theta = 0^\circ, \phi = 180^\circ$	—	200	300	ms		

NOTES:

- The viewing angle is shown in Figure 6.
- Contrast Ratio is defined as follows:

$$C_0 = \frac{\text{Photodetector output voltage with select waveform being applied}}{\text{Photodetector output voltage with non-select waveform being applied}}$$
- The response characteristics of photo-detector output are measured as shown in Figure 7, assuming that input signals are applied so as to select and deselect the dots to be measured, in the optical characteristics test method shown in Figure 11.

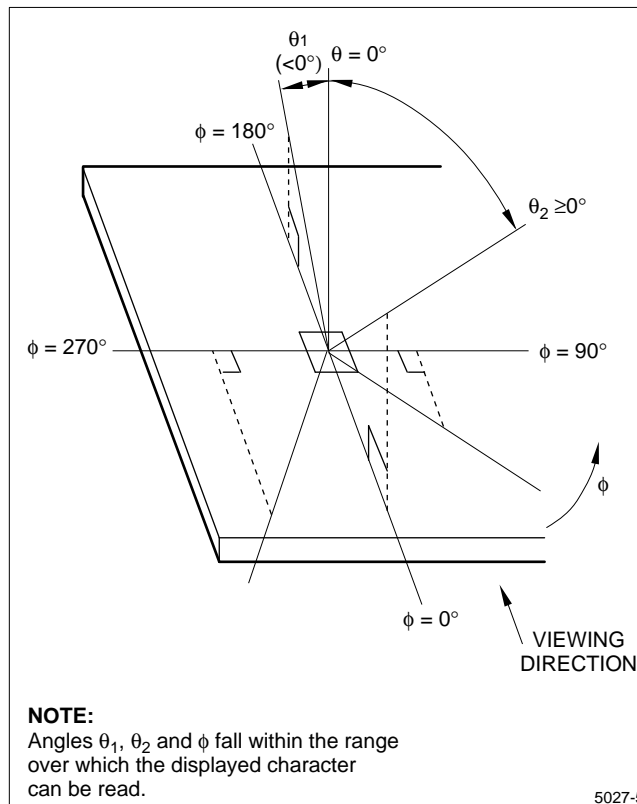
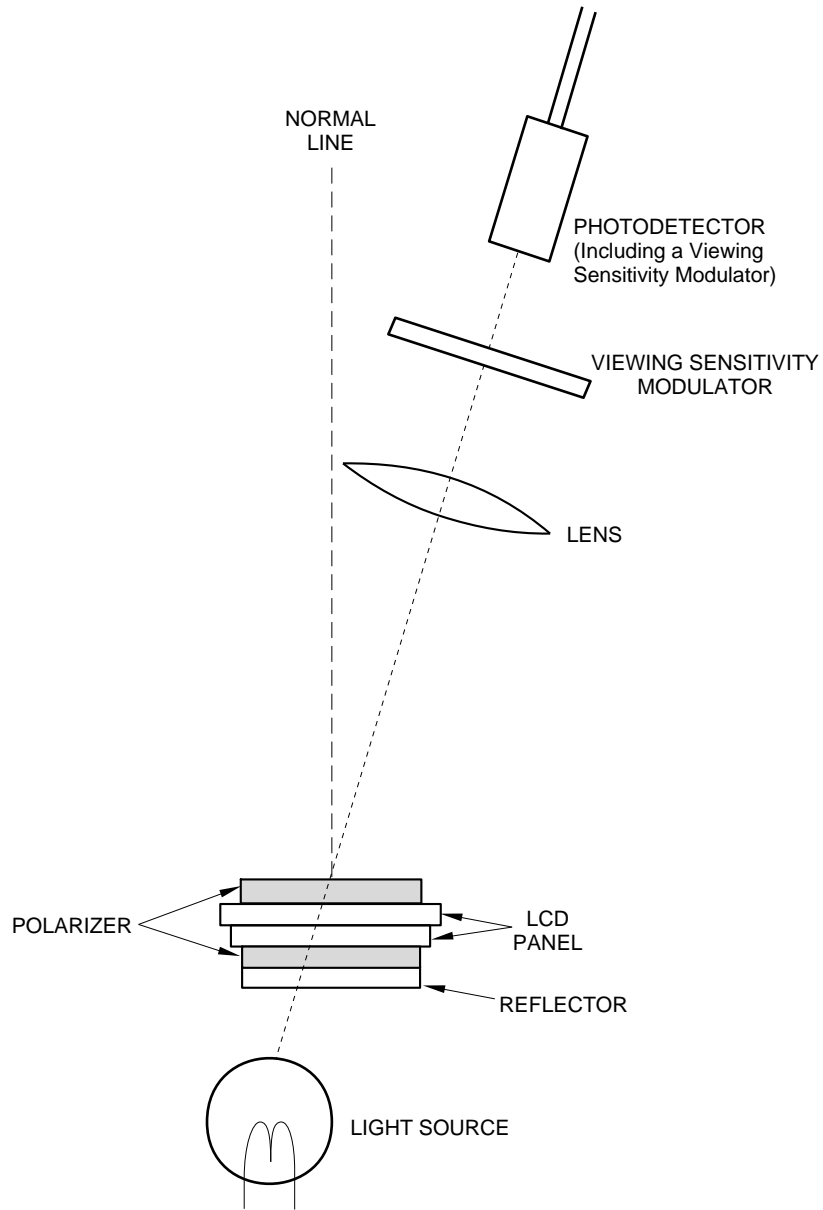


Figure 6. Definition of Viewing Angle



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Figure 7. Optical Characteristics Test Method

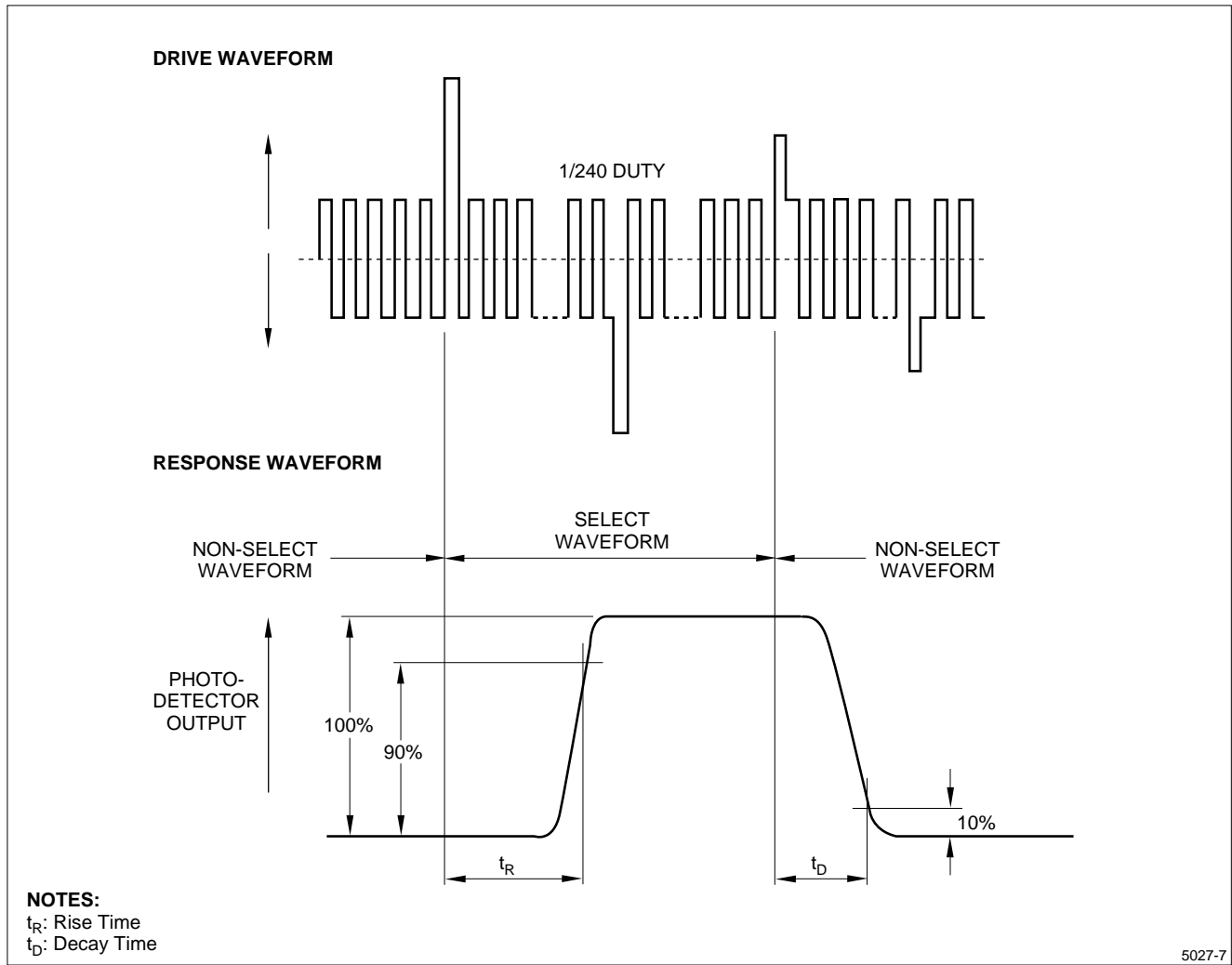


Figure 8. Definition of Response Time

CHARACTERISTICS OF BACKLIGHT

Ratings are defined as the average brightness at five measurement points.

Brightness

PARAMETER	MIN.	TYP.	MAX.	UNIT
Brightness	50	70	–	cd/m ²

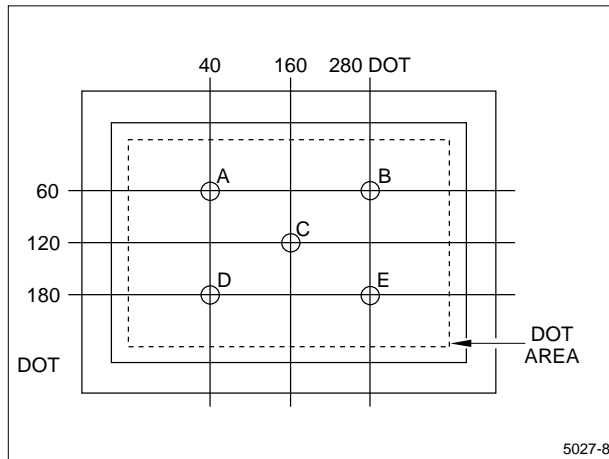


Figure 9. Measuring Points (1 to 5)

Measurement Condition

CCFT Inverter:

LM000106
 INPUT voltage 12.0 V
 IFT = 5 mA

LCD Unit Condition:

LCD is full dot ON (White)
 V_{EE} = -20 V

Temperature:

t_A = 25°C, 30 minutes after turning on.

Measurement Equipment

BM-7 (TOPCON)

Operating Life

The operating lifetime is 10,000 hours or more under the following conditions:

CCFT inverter is LM000106

IFT = 5 mA_{RMS}

t_A = 25 ± 5°C

The operating lifetime is defined as having ended when any of the following conditions are met:

- When the illuminance or quantity of light has decreased to 50% of the initial value.
- When the CCFT flickers.

PRECAUTIONS

- This unit's viewing angle is illustrated in Figure 10 and as follows:
 - $\theta_1 \text{ MIN} < \text{viewing angle} < \theta_2$ ($\theta_1 < 0^\circ$, $\theta_2 \geq 0^\circ$)
 Consider the optimum viewing conditions according to the purpose when installing the unit.

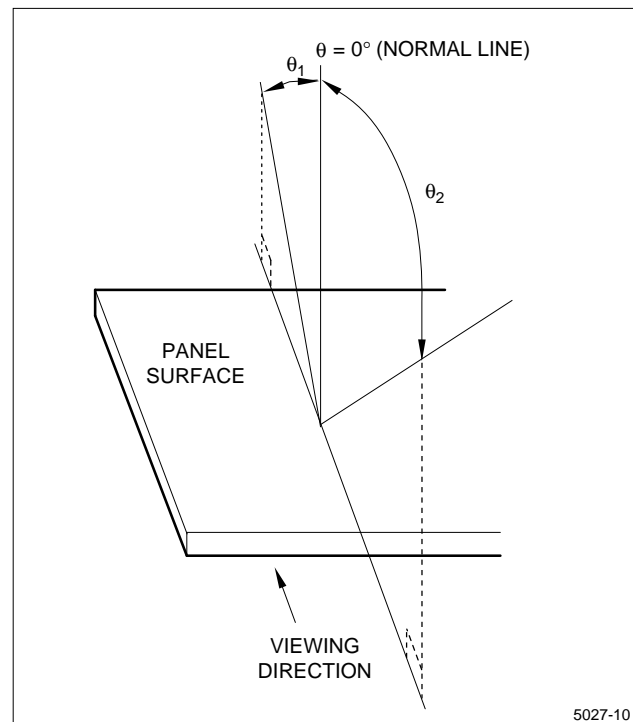


Figure 10. Dot Matrix LCD Viewing Angle

- This unit is installed using mounting tabs at the four corners of PCB or bezel. During installation, avoid undue stress on the unit such as twisting or bending. A transparent acrylic resin board or other type of protective panel should be attached to the front of the unit to protect the polarizer LCD cells, etc.
- Since the front polarizer is easily damaged, use care to not scratch the face.
- If the surface of the LCD cells need cleaning, wipe it with a soft cloth.
- Wipe liquid off immediately since it can cause color changes and staining.
- The LCD is made of glass plates. Use care when handling it to avoid breakage.
- This unit contains CMOS LSIs which are sensitive to electrostatic charges. The following measures should be taken to protect the unit from electrostatic discharge:
 - Ground the metallic case of the main system (contact of the unit and main system).
 - Insulate the unit and main system by attaching insulating washers made of bakelite or nylon.
- The unit should be driven according to the specified ratings to avoid malfunction or permanent damage. DC voltage drive leads to rapid deterioration of LC, so ensure that the drive is alternating waveform by continuous application of the signal M. Avoid latch-up of driver LSIs and application of DC voltage to the LCD panel by following the ON/OFF sequence shown in Figure 11.
- Do not expose the unit to direct sunlight, strong ultraviolet light, etc., for prolonged periods.
- Store the unit at normal room temperature to prevent the LC from converting to liquid (due to excessive temperature changes).
- Do not disassemble the unit.

WARNING: Avoid using any materials which emit gas from epoxy resin (Amines' hardener) and silicon adhesive agent (dealcohol or deoxym) to prevent polarizer color change caused by gas.

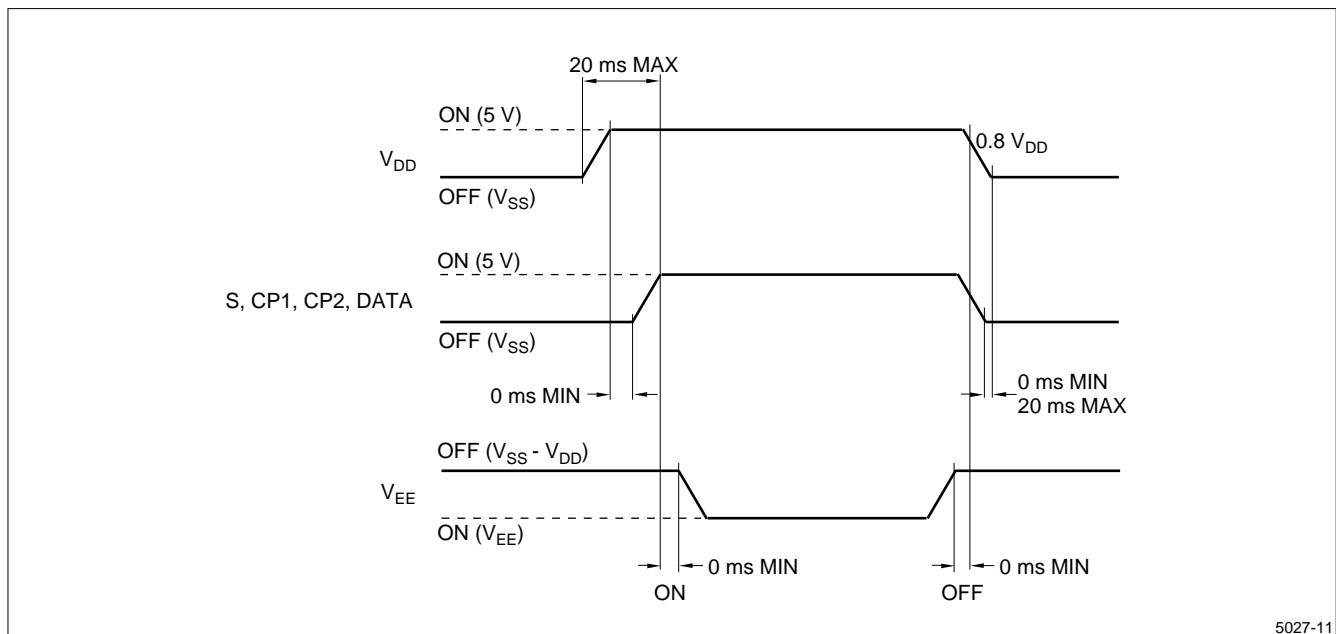


Figure 11. Power ON/OFF Sequence

OUTLINE DIMENSIONS

